ABSTRACT

Each match line of a memory device such as a content addressable memory (CAM) device and a related part of a priority encoder can be separately tested. In test mode, all match lines are first reset/disabled. A write enable pulse signal enables a match line corresponding to a CAM word line at a decoded address to be gated to the priority encoder of the CAM device. The CAM memory storage location and the comparand register are each loaded with the same test entry. A search is performed for the test entry. If the enabled match line is asserted and the priority encoder outputs the address corresponding to the CAM memory storage location, the test is successful. If not there is a match line error or a defect in the priority encoder.